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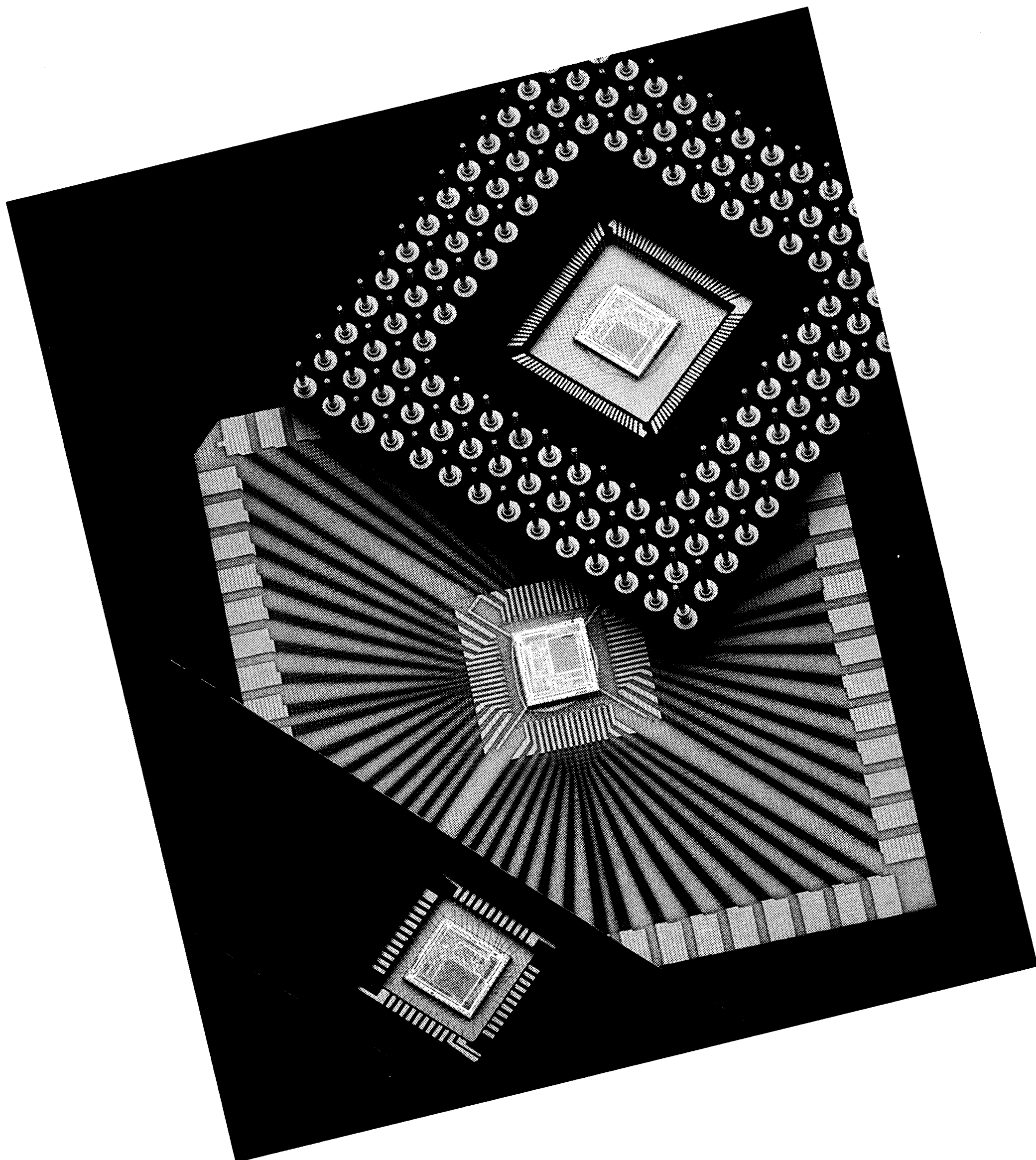
Using the HP 82000 for 1 Gb/s Data Rates

Application Note 398-1



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Introduction

Functional testing of ECL and GaAs digital components, modules, and subsystems may require data rates above one billion bits per second (1 Gb/s). While the HP82000 can be configured to test at rates up to 400 MHz, additional electronics are required for speeds above that rate. Figure 1 illustrates the general concept behind this approach.

Ideally, the added electronics should work closely with existing test system resources so that lower frequency signals can be easily synchronized with higher speed data. The tremendous accuracy and flexibility of the HP82000 makes this feasible.

If the added electronics modules are made up of high speed components (such as ECL or GaAs) then data rates of 1 Gb/s or higher are achievable.

Using the 50 ps edge placement resolution and the per-pin architecture of the HP82000 permits accurate pattern generation at these rates. An example of 1.6 Gb/s patterns is shown in this application note.

Several methods exist for multiplexing test channels to produce these higher rates. Some of these alternatives are also described in this applications note.

Individual high speed channels can be added directly to the DUT performance card for specialized applications.

Alternatively, a modular approach would permit reuse of the high speed circuits. In this case, a portion of the HP82000 pin resources is used to supply data to multiplexing circuits while the rest of the pins are connected directly to the DUT. The interface between the HP82000 and the multiplexers should be flexible enough to permit reuse of the high speed circuits.

Adaptability of the system to a wide variety of digital testing is accomplished by reconfiguring the arrangement of modules and the interface to the DUT. In this way, a trade-off in pin-count vs. speed can be made for maximizing test system resources.

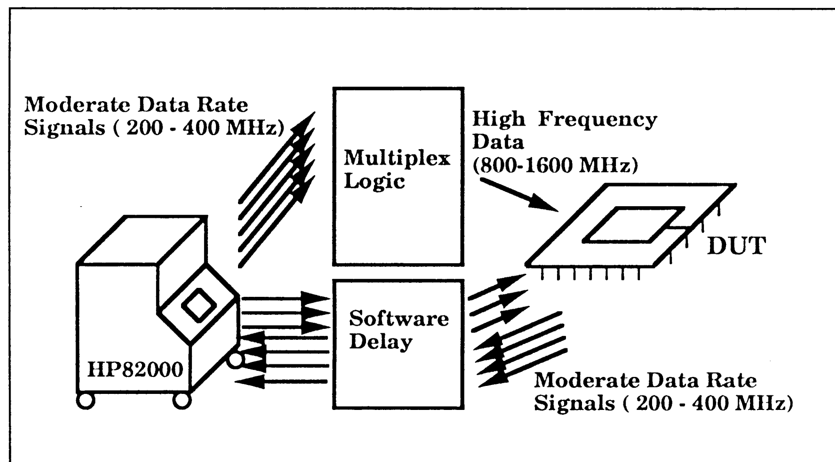


Figure 1:
Use of multiplexing logic for high speed pattern generation.

Parallel Load Shift Registers

In order to generate digital signals for testing at rates above 1 Gb/s, the 200 MHz or 400 MHz data from the HP82000 can be multiplexed. Several possibilities exist for accomplishing the desired combination of data streams. Among these include the use of:

- Parallel load shift registers
- Binary selectable multiplexers
- OR-Gate trees
- Exclusive-OR gate trees

Each of these approaches is described in this application note.

An application which utilizes parallel load shift registers is shown in Figure 2. For this demonstration, standard ECL components were used to build the oscillator, divide-by-3 circuit and shift register. The particular example utilized a much slower, 12.5 MHz test system as the data source. However, the approach could in principle be applied to the higher data rates available with the HP82000.

The circuit accepts a trigger from the test system every 90ns. Using that signal, a burst of 24 clock cycles is generated at 300 MHz as shown in the top trace of Fig.3. This fast clock is used directly by the DUT as well as by additional circuitry to produce the 100 MHz clock shown in the middle trace of Fig.3. The 100 MHz signal is used for testing the DUT as well as for clocking an eight-bit shift register. This register is parallel loaded from the test system during the 10ns "dead" time between bursts and supplies a software programmable bit stream for DUT stimulus. An example of the resulting 100 Mb/s serial bit stream is shown in the lower trace of Fig.3. In this example the pattern 10111010 was applied during the burst.

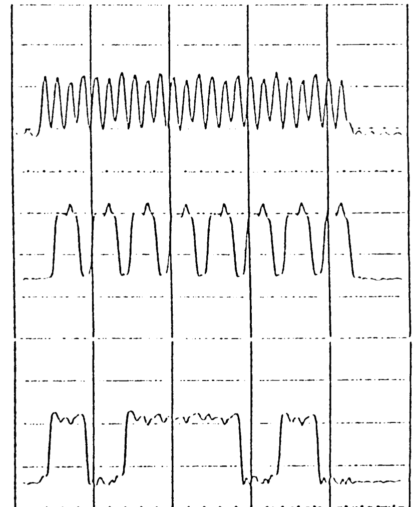


Figure 3:
Performance of (a) a 300 MHz oscillator, (b) 100 MHz clock, (c) 100 Mb/s data

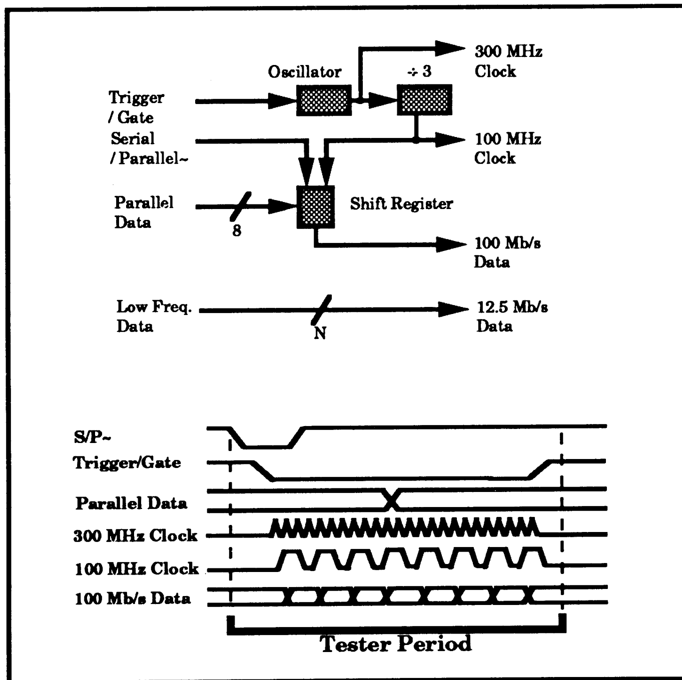


Figure 2:
Parallel loaded shift register for 8:1 multiplexing

It is conceivable that a similar circuit might be constructed using intrinsically faster logic (such as GaAs). However, by taking advantage of the HP82000 "per-pin" resources, much simpler approaches are possible for performing data multiplexing above 1 Gb/s.

Another approach to generating data at high frequencies makes use of combinational logic to form a binary selectable multiplexer. As shown in Figure 4, three select lines (S0, S1, and S2) determine which of the eight data inputs is passed to the circuit output. In this approach, as in the case of the parallel load shift register, the eight input data bits transition only once per tester cycle period while the multiplexer output may switch up to eight times per cycle. By sequencing through the eight possible combinations of the three select lines, each bit is applied once during each cycle for 1/8 the period.

Assuming that a suitable GaAs multiplexer is used, data generation at rates above 1 Gb/s is possible with this method. The difficulty lies with generating and synchronizing the three, high speed, select signals.

First, as in the case of the parallel-load shift register approach, a high frequency clock signal must be generated which is synchronous with the HP82000 vector cycle. Alternatively, the HP82000 could be externally clocked by a divided down derivative of the high frequency signal.

Secondly, the high frequency clock must be divided down to produce the other two select signals. This can be accomplished with a simple GaAs binary counter.

In addition, each of the select signals must be accurately timed (to within a fraction of a nanosecond) and distributed to the multiplexers. The eight input data bits must also be timed properly. However, the HP82000 timing per pin capability can be exploited to provide wider timing margins by staggering the input phase relationships.

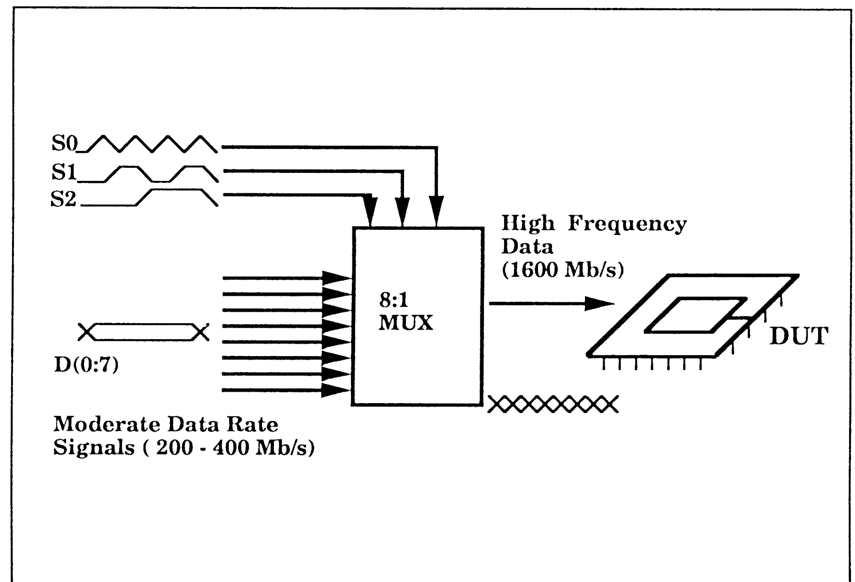


Figure 4:
Timing and block diagram for a binary selectable multiplexer

Both methods described above require that high speed clock and control signals be generated in addition to parallel data. Furthermore, for multiple channels, several high speed clock signals must be generated to allow independent control of channel-to-channel skew (both for calibration and offset).

In dealing with very high frequency signals it is usually best to minimize the complexity of the controlling circuitry as much as is possible while still providing the required function. By leveraging the high timing precision available with the HP82000, it is possible to simplify the multiplexing logic even further.

One of the simplest methods for combining data streams uses a multiple input OR gate or an OR gate "tree" as depicted in Figure 5. In this example the four data streams are phase delayed by 1/4 the tester period such that only one bit from one data stream is valid at any given time. When the data is not valid, the use of Return-to-Zero format insures that valid data is passed directly through the OR gate tree.

The advantages of this approach are (1) that continuous bit streams can be generated at up to four times the vector rate and four times the memory depth of the test system and (2) that timing edge placement is directly controlled by the tester.

However, the OR gate tree method suffers from a difficulty in precisely placing the timing edges. These must be placed such that there is no significant overlap between valid data bits. On the other hand, edges must be placed such that one data bit is valid at all times (to avoid glitches and "dead" times). Specifically, the leading edge of one signal must precisely coincide with the trailing edge of another.

Even when inputs to the OR tree are programmed to meet these demanding requirements, partial transitions may occur between consecutive "high" bits. Examples of such undesirable results are shown in Figure 6b and Figure 6c.

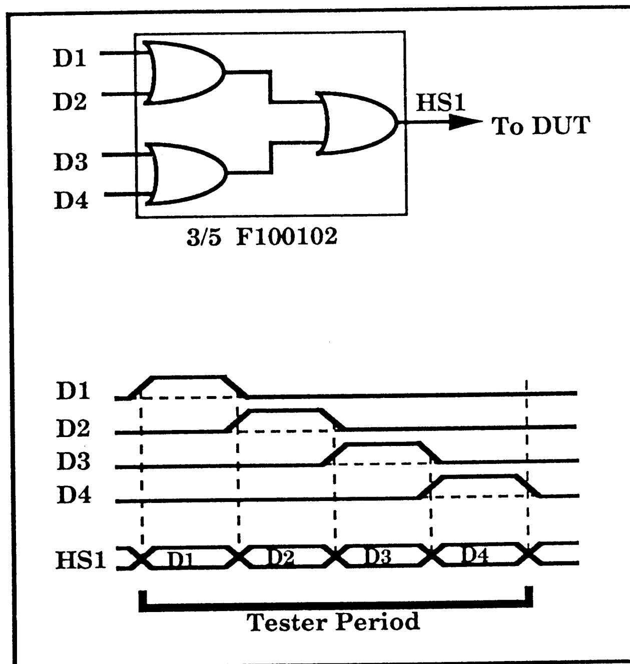


Figure 5:
OR-Gate tree for
4:1 multiplexing

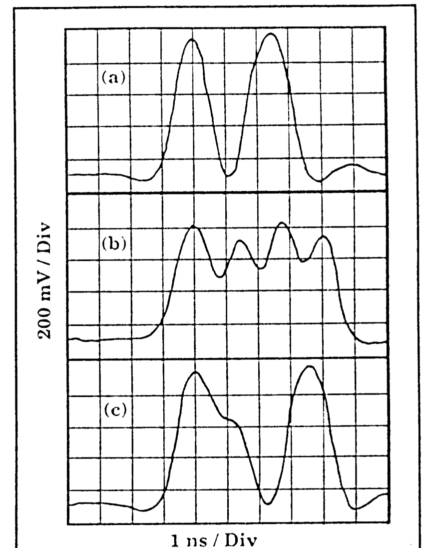


Figure 6:
800 Mb/s patterns from a
4:1 ECL OR-Gate tree;
(a) 1010, (b) 1111, (c) 1101

Exclusive OR Gate Tree

A method for combining data streams which uses a multiple input exclusive-OR gate "tree" is shown in Fig.7. For these experiments, the XOR tree was made up of GigaBit Logic digital GaAs components. The output of the GaAs logic was used to supply high frequency data to a GaAs pin driver (GigaBit Logic 16G061A). This device has voltage programmable high and low logic levels to permit high speed noise margin testing. Logic transitions (both low-to-high and high-to-low) occur in about 250 picoseconds (20-80%) thereby permitting the generation of gigabit per second data rates.

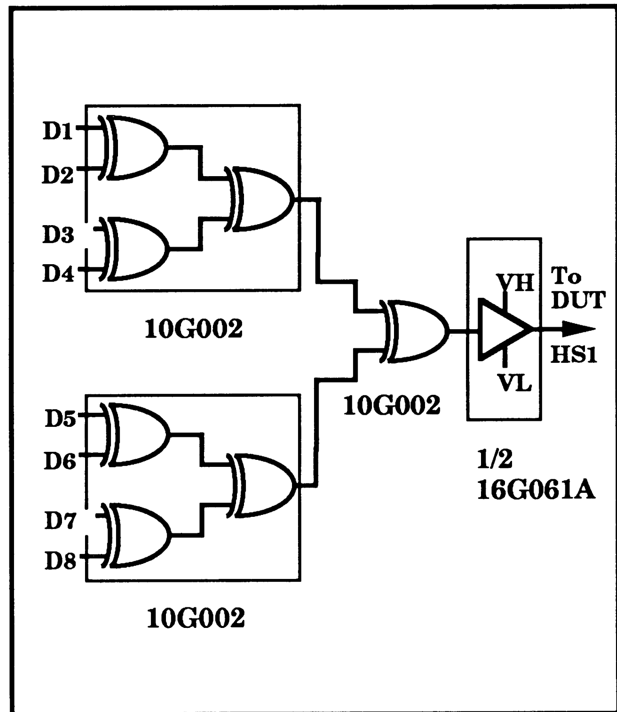


Figure 7: XOR tree for 8:1 multiplexing

The static logic of the XOR tree is such that a transition on any input will result in a change in the output state. This fact can be exploited if the input timing is staggered so that only one channel changes state at a time. Specifically, the eight data streams are phase delayed in increments of 1/8 the tester period as shown in Figure 8.

If the data on all eight channels is properly coded, then any desired bit stream can be generated at eight times the input data rate. In effect, the coded data is decoded in real time by the XOR tree.

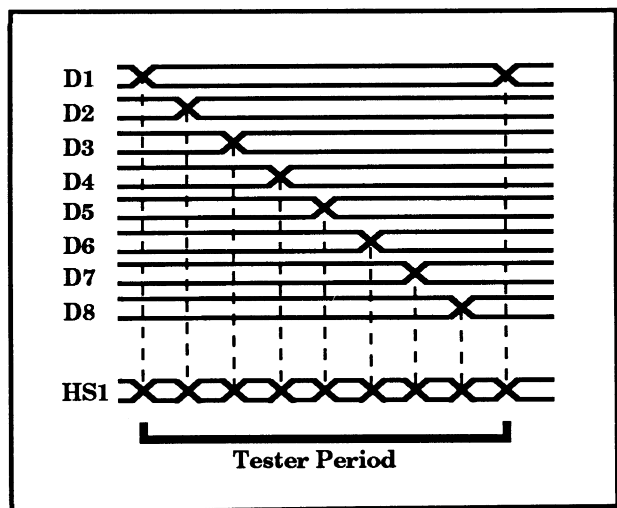


Figure 8: Timing for the 8:1 GaAs XOR multiplexer

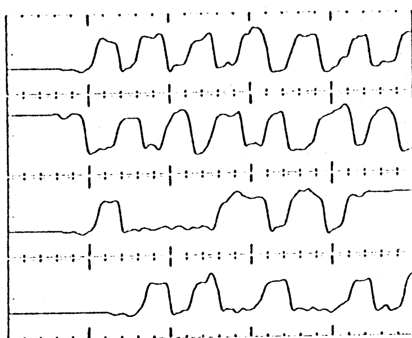
The HP82000 used for these experiments provides independent control of timing on a "per-pin" basis with 50 ps edge placement resolution. This high degree of timing resolution is essential for accurate placement of transition edges at 1 Gb/s rates.

Example : GaAs XOR Tree

Several examples of high speed data patterns are shown in Figure 9. For these signals, eight 200 Mb/s channels were used to supply data to the GaAs XOR tree. The resulting 1.6 Gb/s logic signals are displayed in the figure. In the top trace an alternating series of 1's and 0's is produced to generate an 800 MHz clock signal. The second trace is an inverted clock. The third and fourth signals are arbitrary data patterns at 1.6 Gb/s.

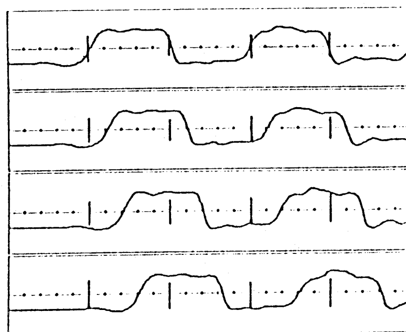
An example of the timing precision which can be achieved with this approach is shown in Figure 10. Here an eight input XOR tree produced an alternating pattern of "01010..." at a rate of 1.0Gb/s. In the top trace, it can be seen that the logic transitions are evenly spaced at intervals of 1ns (within about 50 ps). For the second trace, the input timing for all eight channels was programmed with an additional 200ps delay. The resulting waveform shows accurate positioning of the delayed edges. The third and fourth traces in the figure show examples of 400ps and 600ps delayed signals respectively.

Using the GigaBit Logic 16G061A pin driver, the logic high and low levels may be independently programmed. Figure 11 shows an example of several pulses with low levels at -2.0V and high levels ranging between -1.0V and +1.0V in 0.5V increments. The nominal pulse width ranged between 1.5ns and 2.0ns. However, no attempt was made in this example to maintain a constant width.



2 ns / Div

Figure 9 :
1.6 Gb/s data generated using a GaAs XOR tree



1 ns / Div

Figure 10 :
200 ps incremental delays of a 1.0 Gb/s pattern

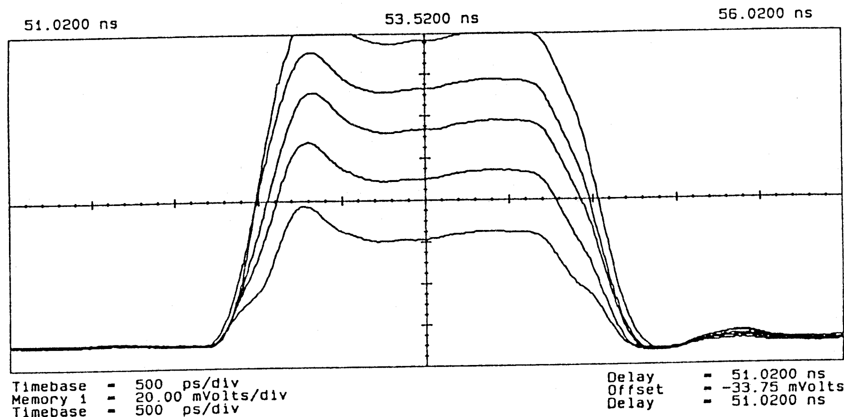


Figure 11 :
Examples of logic level programmability

In each of the methods used for multiplexing test system channels, timing and voltage calibration is critical. Clearly for the resulting high speed signal to be accurately timed the input signals must be placed at least as accurately. By utilizing the HP82000 50 ps edge placement resolution, timing edges can be adjusted to compensate for errors which may result from differences in cable lengths or differences in propagation delays through the multiplexing logic.

However, one source of timing error which is not easily corrected is due to pulse width distortions occurring in multiplexing logic. Specifically, if the effective input threshold of the multiplexer is higher than or lower than the 50% point of the test system logic levels, then a positive going pulse will be either shortened or lengthened respectively. Clearly, any appreciable pulse width distortion will have an adverse effect on the high speed signals generated by the multiplexer.

An example of pulse narrowing due to logic level mismatch is shown in Figure 12. Here an 8.0ns pulse from the HP82000 is shown in the top trace. The bottom signal is the resulting output of a GaAs multiplexer. The measured width of the pulse is 7.80ns, or 200ps shorter than desired.

In this example, the effective threshold of the GaAs gate was about 100mV lower than the 50% logic level of the signal from the HP82000. Because the test system logic transitions have a slew rate of about 1V/ns at these levels, the pulse is shortened by about 100ps at both the leading and trailing edges. This accounts for the observed pulse distortion.

While we cannot easily adjust the GaAs input threshold, we do have control over the logic levels of the signals from the HP82000. Furthermore, because the HP82000 levels are programmable on a per pin basis, we can compensate for this type of pulse width distortion for all inputs to the GaAs multiplexer.

Figure 13 shows the results of lowering the HP82000 logic levels by 100mV as compared with Figure 12. The resulting output is now 7.96ns wide (within 40ps of the desired width).

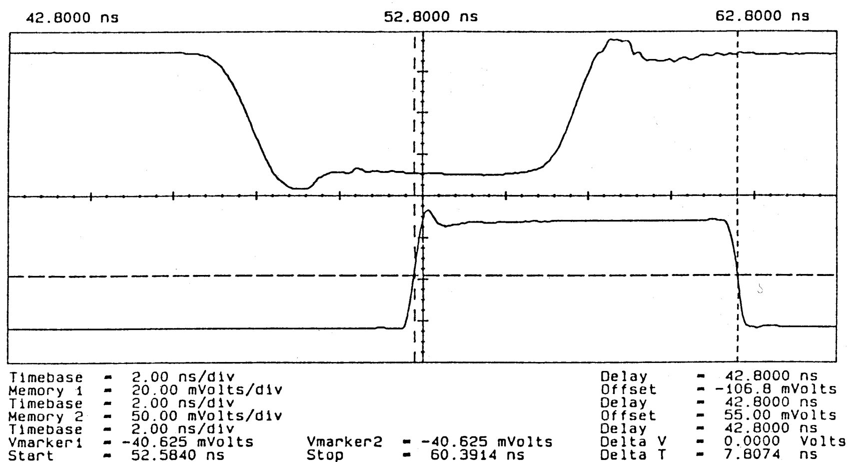


Figure 12:
Pulse width distortion due to mismatch between the tester and GaAs logic.

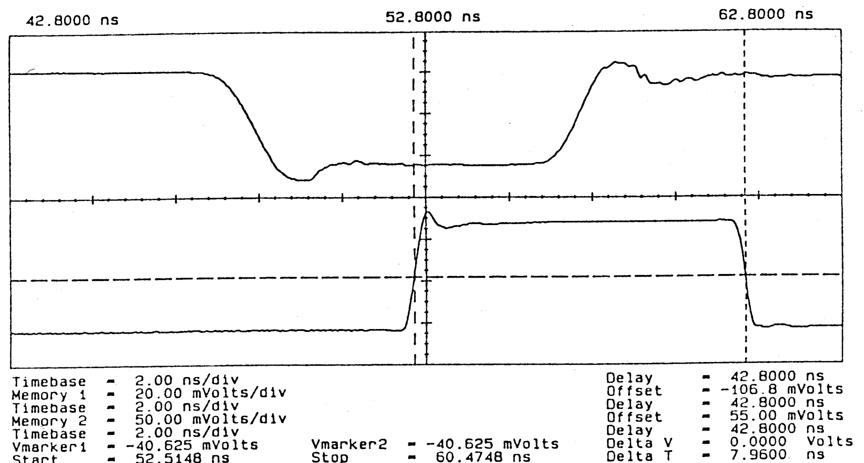


Figure 13:
Correction for pulse width distortion

A conceptual drawing of a modular, high speed digital test system is shown in Fig.14. The outer border represents the high speed test head of the HP82000 system. The pogo interface is represented by the array of arrows in the drawing. These pins are arranged in a rectangular grid with each high speed signal surrounded by two ground pins. This arrangement helps to maintain the 50 Ohm transmission line impedance and to preserve signal quality at frequencies up to 200 MHz. Cross talk is also reduced. Test system programmable power supplies are also routed through this interface.

Normally tester signals are connected through the pogo pins to the bottom side of the DUT "performance board". This customized printed circuit board is designed to connect tester signals to the appropriate device socket pins. A modified DUT performance board is shown on the right side of the figure.

Six of the DUT pins are connected through microstrip traces to SMA connectors mounted on the left edge of the board. Coaxial cables are used to link to electronic modules on the Ultra High Frequency PCB. Each of these modules support the multiplexing of several (4 or 8) tester channels to provide data at rates above 200 Mb/s. The modular approach permits the re-use of several different high speed circuits. Various specialized functions could be supported in addition to the general purpose multiplex functions described here. The system may accommodate specific test requirements by rearranging or replacing the modules and coaxial cables.

The DUT outputs can be monitored directly by the existing tester comparators using a multi-pass test method. The edge-strobe mode is used with the strobe phase set to monitor one of the bits produced during each tester cycle. During successive passes, the strobe timing is delayed so that it monitors the later occurring bits, one at a time. High speed DUT outputs are sampled in this multi-pass mode directly by the HP82000 2 GHz bandwidth comparators.

Alternatively, DUT output signals may be monitored by multiple comparators. Above about 600 to 700 Mb/s, however, multipass and multiple comparator sampling is likely to be ineffective. In this case, DUT outputs must be demultiplexed, with the parallel signals sampled by multiple comparators.

Conclusions

In this applications note, we have examined several methods which may be applied to high speed digital testing with the HP82000. This list, while not exhaustive, is representative of the options available. The optimal method will depend on the specific test requirements of the DUT and other economic considerations.

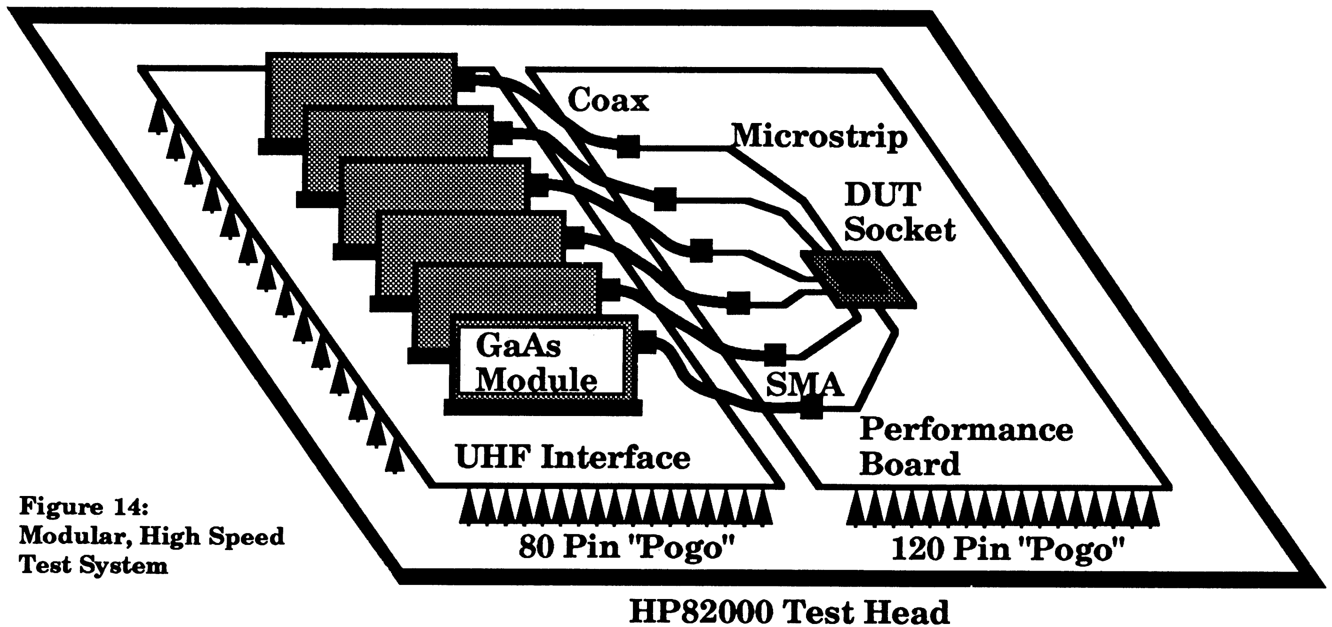


Figure 14: Modular, High Speed Test System

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